



# NCP5050

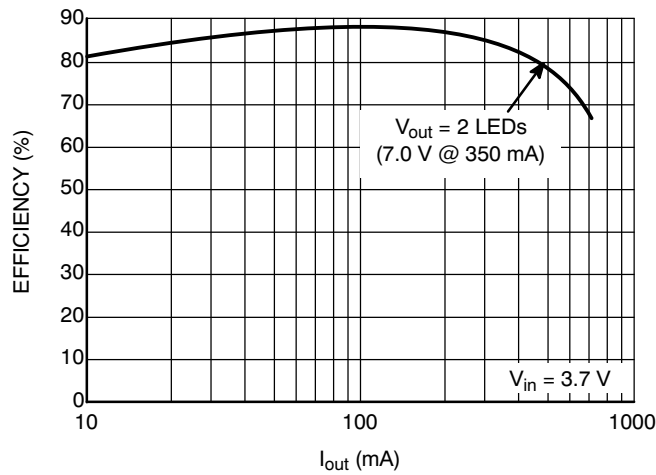


Figure 2. Typical Efficiency

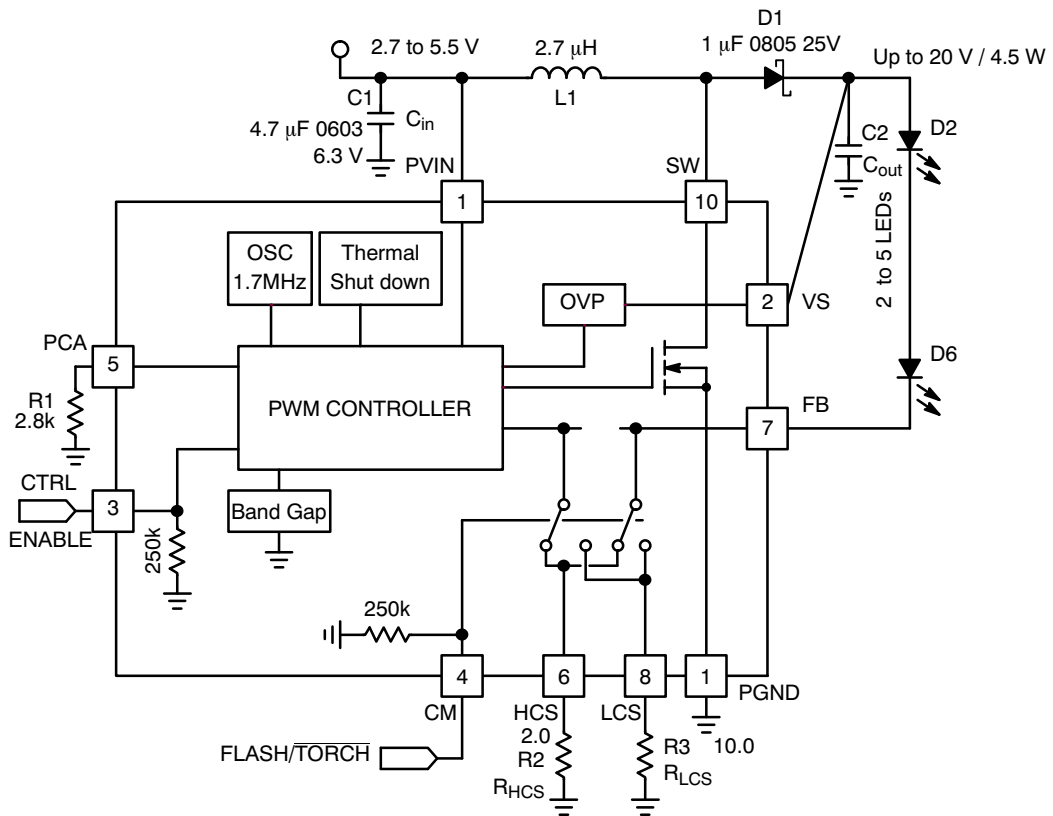


Figure 3. Simplified Block Diagram

## NCP5050

### PIN FUNCTION DESCRIPTION

| Pin | Pin Name | Type  | Description   |
|-----|----------|-------|---|
| 1   | PGND     | POWER | <b>Power Ground:</b> This pin is the power ground and carries the high switching current. A high quality ground must be provided to avoid any noise spikes/uncontrolled operation. Cares must be observed to avoid high-density current flow in a limited PCB copper track.   |
| 2   | VS       | INPUT | <b>Voltage Sense:</b> In order to sense $V_{out}$ notably for over voltage protection, this input must be connected to the output bypass capacitor $C_{out}$ .  |
| 3   | CTRL     | INPUT | <b>Control and Enable:</b> An active high logic level on this pin enables the device. A built-in pulldown resistor disables the device if the pin is left open. Also in disable condition the device provide a true cut-off thank to the high impedance on FB input. This pin can also be used to control the average current into the load by applying a low frequency PWM signal. If a PWM signal is applied, the frequency should be high enough to avoid optical flicker but be no greater than 50 kHz. |
| 4   | CM       | INPUT | <b>Current Mode:</b> An active high logic on this input enables the High Current Sense used for flash and disables the LCS resistor. This pin has a low voltage threshold so it can be driven directly from 1.8 V logic signals. If this function is not needed, this pin should be grounded. Only when CM pin is high, a safety function switch off the output if CTRL pin is high longer than 1.2 s   |
| 5   | PCA      | INPUT | <b>Peak Current Adjust:</b> A resistor between this input and ground controls the maximum peak current allowed in the inductor. The minimum value for this resistor is 2.8 k $\Omega$ and increasing this value decreases the peak current. This allows the user to adjust the current based on the application needs and scale the size of the inductor accordingly. See "Switch Current Limit" guidelines in application section.   |
| 6   | HCS      | INPUT | <b>High Current Sense:</b> This pin is used for Flash Mode. If the user desires two levels of LED current then a resistor should be connected from this pin to ground. This function is controlled by the CM input.   |
| 7   | FB       | INPUT | <b>Feedback:</b> The reference is 250 mV. This pin provides the feedback voltage by means of the sense resistors fixed by LCS or HCS pin. When the device is enables and CM low, the LCS resistor is connected to this pin, thereby the LCS setup the LED current. The tolerance of the LED current is dependant upon the accuracy of this sense resistor and a $\pm 1\%$ metal film resistor, or better, is recommended for best output accuracy.  |
| 8   | LCS      | INPUT | <b>Low Current Sense:</b> This pin is used for Torch Mode. In order to fix the current when CM logic pin is low, a resistor should be connected from this pin to ground.  |
| 9   | PVIN     | POWER | <b>Power Supply:</b> The external voltage supply is connected to this pin. A 4.7 $\mu$ F / 6.3 V high quality capacitor must be connected across this pin and the power ground to achieve the specified output power parameters. The X5R low $\Delta$ C/C versus DC bias ceramic types are highly recommended.  |
| 10  | SW       | INPUT | <b>Switch:</b> Power switch connection for inductor. Typical application will use a coil from 2.2 $\mu$ H – 4.7 $\mu$ H and must be capable of handling the peak current.   |

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## MAXIMUM RATINGS (Note 1)

| Rating   | Symbol                                      | Value                                  | Unit                    |
|--|---|--|-------------------------|
| Power Supply Voltage (Note 2)  | $P_{Vin}$                                   | 7.0                                    | V                       |
| Over Voltage Protection  | $V_S$                                       | 25                                     | V                       |
| Human Body Model (HBM) ESD Rating (Note 3)<br>HCS and FB Pins  | ESD HBM                                     | 2000<br>1000                           | V                       |
| Machine Model (MM) ESD Rating (Note 3)<br>HCS and FB Pins  | ESD MM                                      | 200<br>150                             | V                       |
| Digital Input Voltage<br>Digital Input Current   | CTRL, CM                                    | $-0.3 < V_{in} < V_{bat} + 0.3$<br>1.0 | V<br>mA                 |
| WDFN 3x3 Package<br>Power Dissipation @ $T_A = +85^\circ\text{C}$<br>Thermal Resistance, Junction-to-Case<br>Thermal Resistance, Junction-to-Air | $P_D$<br>$R_{\theta JC}$<br>$R_{\theta JA}$ | (Note 5)<br>10<br>(Note 6)             | W<br>$^\circ\text{C/W}$ |
| Operating Ambient Temperature Range  | $T_A$                                       | -10 to +85                             | $^\circ\text{C}$        |
| Operating Junction Temperature Range   | $T_J$                                       | -10 to +125                            | $^\circ\text{C}$        |
| Maximum Junction Temperature   | $T_{JMAX}$                                  | +150                                   | $^\circ\text{C}$        |
| Storage Temperature Range  | $T_{stg}$                                   | -65 to +150                            | $^\circ\text{C}$        |
| Moisture Sensitivity Level (Note 7)  | MSL   | 1                                      |                         |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- Maximum electrical ratings are defined as those values beyond which damage to the device may occur at  $T_A = 25^\circ\text{C}$ .
- According to JEDEC standard JESD22-A108B.
- This device series contains ESD protection and passes the following tests:  
Human Body Model (HBM) per JEDEC standard: JESD22-A114 for all pins.  
Machine Model (MM) per JEDEC standard: JESD22-A115 for all pins.
- Latch up Current Maximum Rating:  $\pm 100$  mA per JEDEC standard: JESD78.
- The thermal shutdown set to  $160^\circ\text{C}$  (typical) avoids irreversible damage on the device due to power dissipation.
- For the 10-Pin 3x3 WDFN Package, the  $R_{\theta JA}$  is highly dependent on the PCB heat-sink area. For example,  $R_{\theta JA}$  can be  $61^\circ\text{C/W}$  for 2 layers board having  $51\text{ mm}^2$  dissipation area on circuit side and board size ground plane on other side.
- Per IPC/JEDEC standard: J-STD-020A.
- The maximum package power dissipation limit must not be exceeded.

$$P_d = \frac{125 - T_A}{R_{\theta JA}}$$

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**ELECTRICAL CHARACTERISTICS** Minimum and Maximum Limits apply for  $T_A$  between  $-10^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  and  $V_{IN}$  between 2.7 V to 5.5 V (Unless otherwise noted). Typical values are referenced to  $T_A = +25^{\circ}\text{C}$  and  $V_{in} = 3.6\text{ V}$  (Unless otherwise noted)

| Characteristics  | Symbol          | Min        | Typ    | Max    | Unit               |
|--|-----------------|------------|--------|--------|--------------------|
| Operating Power Supply   | $V_{in}$        | 2.7        | -      | 5.5    | V                  |
| Maximum Inductor Current (Notes 9 and 11) (see Figure 24)<br>Refer Switch Current Limit section @ $25^{\circ}\text{C}$ | $I_{PEAK\_MAX}$ | 1.0        | -      | 3.0    | A                  |
| Power Switch ON Resistor<br>$T_A = 25^{\circ}\text{C}$ ( $I = 100\text{ mA}$ )   | $SWR_{DSON}$    | -          | 200    | -      | $\text{m}\Omega$   |
| High Current Sense Switch ON Resistor ( $I = 100\text{ mA}$ and $25^{\circ}\text{C}$ )                                 | $HCSSR_{DSON}$  | -          | 250    | -      | $\text{m}\Omega$   |
| Low Current Sense Switch ON Resistor ( $I = 100\text{ mA}$ and $25^{\circ}\text{C}$ )                                  | $LCSSR_{DSON}$  | -          | 750    | -      | $\text{m}\Omega$   |
| PWM Oscillator Frequency   | $F_{OSC}$       | 1.48       | 1.7    | 1.95   | MHz                |
| Maximum Duty Cycle   | $M_{DUTY}$      | 91.5       | 94     | -      | %                  |
| Efficiency (Notes 9 and 10)  | $E_{FF}$        | 85         | 90     | -      | %                  |
| Over-voltage Clamp Voltage   | $OVP_{ON}$      | 20         | -      | -      | V                  |
| Over-voltage Clamp Hysteresis  | $OVP_H$         | -          | 1.0    | -      | V                  |
| Output power (Notes 9 and 12)<br>@ $V_{in} = 3.3\text{ V}$<br>@ $V_{in} = 2.7\text{ V}$                                | $P_{out}$       | 4.5<br>2.8 | -<br>- | -<br>- | W                  |
| Feedback Voltage Ripple Rejection @ $I_{out} = 20\text{ mA}$<br>From DC to 300 Hz (0.2 $V_{PP}$ ) (Note 9)             | $L_{REG}$       | 5.0        | 2.5    | -      | mV                 |
| Feedback Voltage in Steady State @ $T_A = 25^{\circ}\text{C}$  | $F_{BV}$        | 215        | 250    | 285    | mV                 |
| Input Feedback Current (CM = Low)  | $I_{FB}$        | -          | -      | 0.15   | $\mu\text{A}$      |
| $V_{in}$ Undervoltage Lockout<br>$V_{in}$ Decreasing   | $UV_{LO}$       | 2.0        | -      | 2.7    | V                  |
| Undervoltage Lockout Hysteresis  | $UV_{LOH}$      | -          | 100    | -      | mV                 |
| Standby Current, $I_{out} = 0\text{ mA}$ , CTRL = Low, $V_{in} = 4.2\text{ V}$ @ $T_A = 25^{\circ}\text{C}$            | $I_{STDB}$      | -          | -      | 2.0    | $\mu\text{A}$      |
| Quiescent Current, $I_{out} = 0\text{ mA}$ , Not Switching @ $T_A = 25^{\circ}\text{C}$                                | $I_{QNOSW}$     | -          | -      | 2.0    | mA                 |
| Startup Time (Note 9)<br>From CTRL = 1.2 V to Start of Switching   | $STRT$          | -          | 50     | 200    | $\mu\text{s}$      |
| Inrush Peak Current Limit (Note 9)<br>Time Constant  | $I_{PCL}$       | -          | 1      | -      | ms                 |
| Upper Limit of PWM Dimming Frequency (Note 9)  | $D_{IM}$        | -          | -      | 50     | kHz                |
| Time out Protection (Note 9)   | $T_{OUT}$       | -15%       | 1.2    | +15%   | s                  |
| Thermal Shutdown Protection (Note 9)   | $T_{SD}$        | -          | 160    | -      | $^{\circ}\text{C}$ |
| Thermal Shutdown Protection Hysteresis (Note 9)  | $T_{SDH}$       | -          | 20     | -      | $^{\circ}\text{C}$ |
| Voltage Input Logic Low (Pin CM, CTRL)   | $V_{IL}$        | -          | -      | 0.4    | V                  |
| Voltage Input Logic High (Pin CM, CTRL)  | $V_{IH}$        | 1.2        | -      | -      | V                  |
| CTRL and CM Pin Pulldown Resistance  | $R_{PLD}$       | 175        | 250    | 375    | $\text{k}\Omega$   |

9. Guaranteed by design and characterized

10. Efficiency is defined by  $100 * (P_{out} / P_{in})$  at  $25^{\circ}\text{C}$

$V_{in} = 4.2\text{ V}$ , L = TDK VLF5014A-2R7M1R5

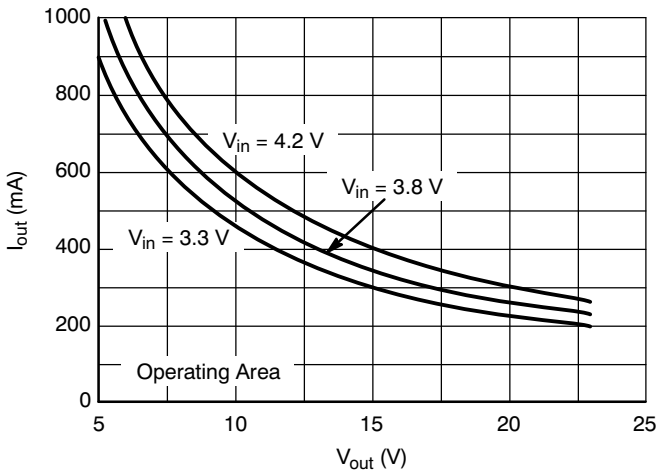
Load = 80 mA, 4 LED ( $V_F = 3.5\text{ V}$  per LED,  $C_{out} = 1\text{ }\mu\text{F X5R}$ )

11. The overall tolerance is dependent on the accuracy of the external resistor. A 1% tolerance metal film resistor is recommended to achieve  $I_{PEAK\_MAX} \pm 20\%$  accuracy.

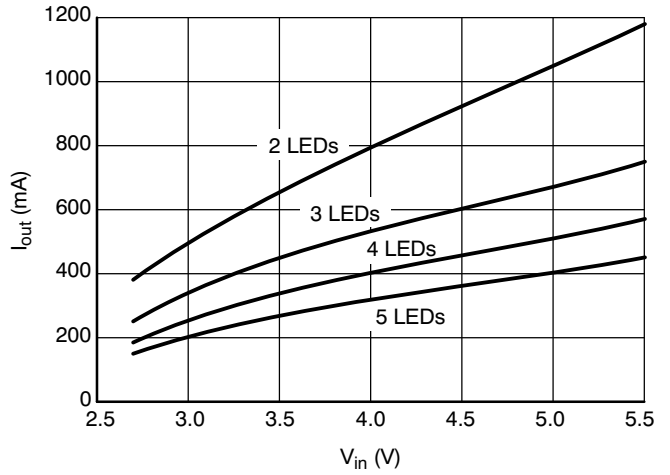
12. With Schottky diode MBR130LSF and TDK VLF5014A-2R7M1R5 inductor.

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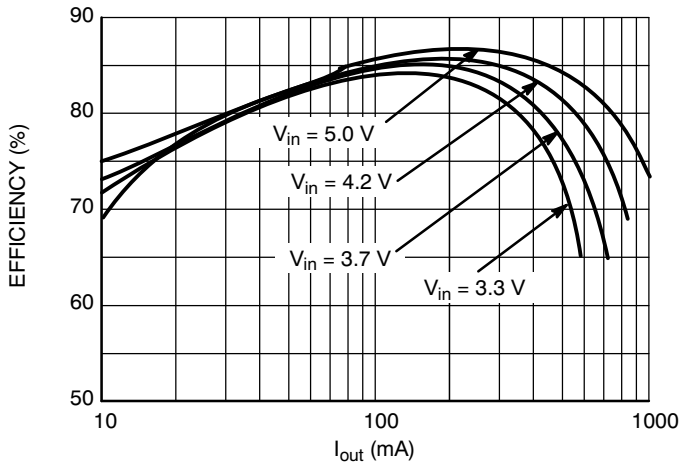
## TYPICAL OPERATING CHARACTERISTICS



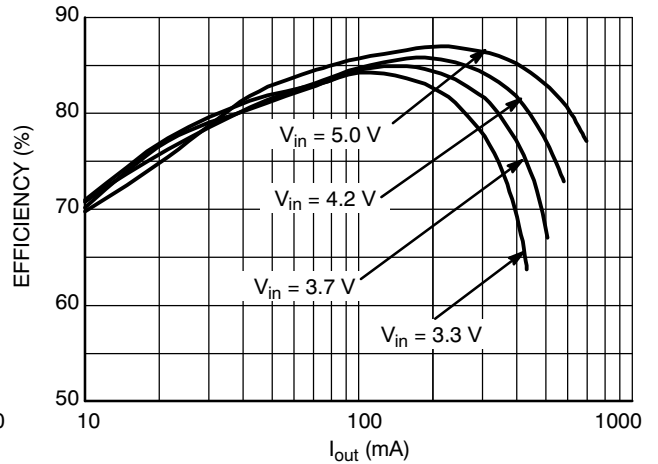
**Figure 4. Maximum Output Current Available vs.  $V_{out}$**



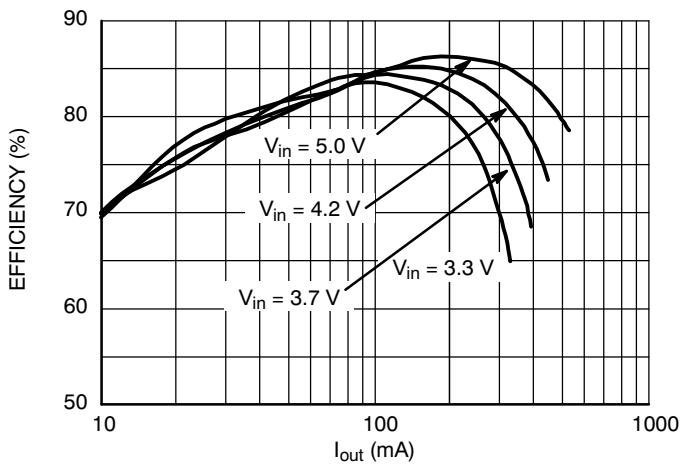
**Figure 5. Typical Maximum Output Current vs. Input Voltage, L = TDK VLF5014A-2R7M1R5 (Note 13)**



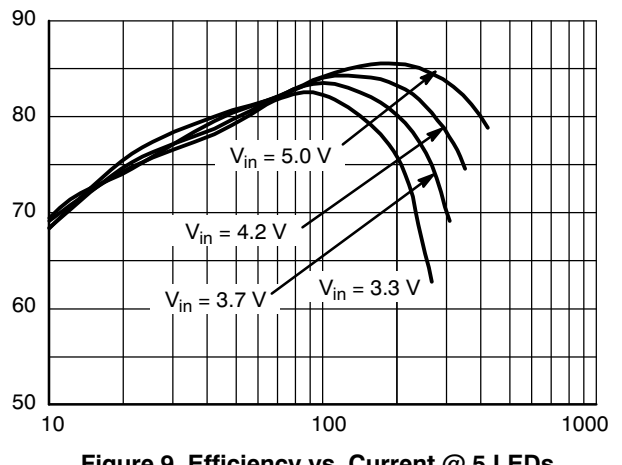
**Figure 6. Efficiency vs. Current @ 2 LEDs (7.0 V @ 350 mA), L = TDK VLF5014A-2R7M1R5, (Notes 13 and 14)**



**Figure 7. Efficiency vs. Current @ 3 LEDs (10.5 V @ 350 mA), L = TDK VLF5014A-2R7M1R5, (Notes 13 and 14)**



**Figure 8. Efficiency vs. Current @ 4 LEDs (14 V @ 350 mA), L = TDK VLF5014A-2R7M1R5, (Notes 13 and 14)**



**Figure 9. Efficiency vs. Current @ 5 LEDs (17.5 V @ 350 mA), L = TDK VLF5014A-2R7M1R5 (Notes 13 and 14)**

13. Pulse of 500 ms every 3 s in Flash Mode (Current following through HCS pin).

14. Efficiency =  $100 \times (\text{Number of LED stacked} \times V_{LED} \times I_{LED}) / P_{in}$ .

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## TYPICAL OPERATING CHARACTERISTICS

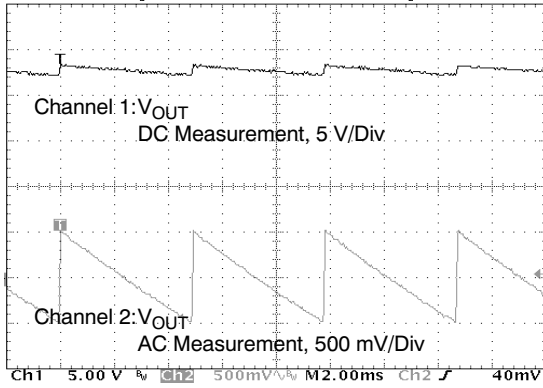


Figure 10. Typical  $V_{OUT}$  Ripple in OVP Condition, No Load

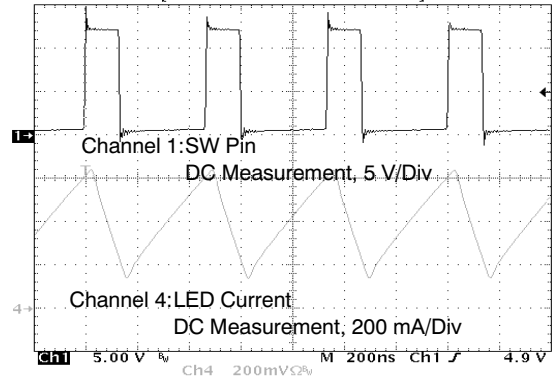


Figure 11. Continue Current Mode (CCM),  $I_{OUT} = 100 \text{ mA}$

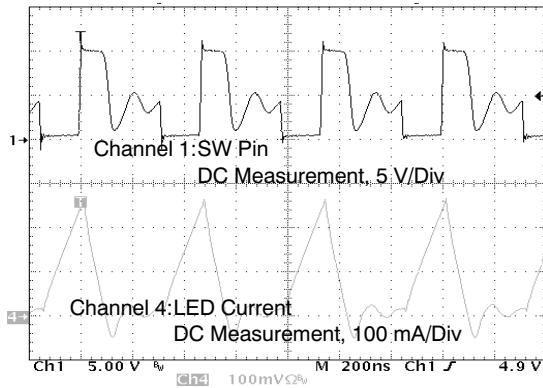


Figure 12. Discontinuous Current Mode (DCM),  $I_{OUT} = 20 \text{ mA}$

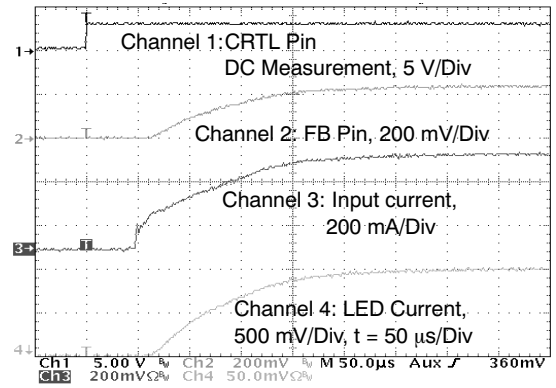


Figure 13. Startup for 3 LEDs Operating,  $I_{LEDs} = 100 \text{ mA}$ ,  $R_{sense} = 2.5 \Omega$

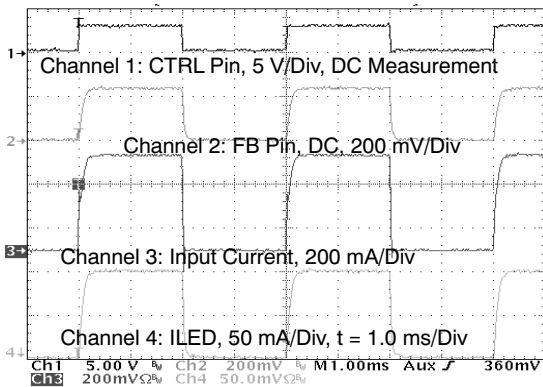


Figure 14. Low Frequency Dimming Control,  $F = 250 \text{ Hz}$

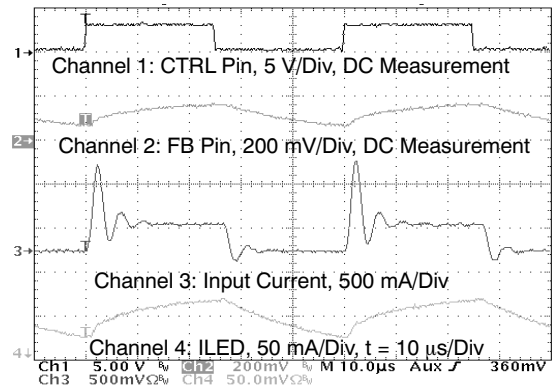


Figure 15. High Frequency Dimming Control,  $F = 20 \text{ kHz}$

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## TYPICAL OPERATING CHARACTERISTICS

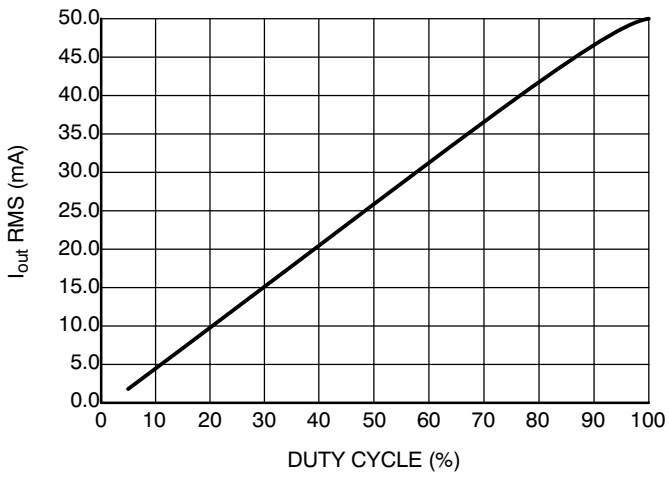


Figure 16. Dimming on CTRL:  $I_{OUT\ RMS}$  vs. Duty Cycle  $R_{BF} = 5\ \Omega$ ,  $F = 20\ kHz$

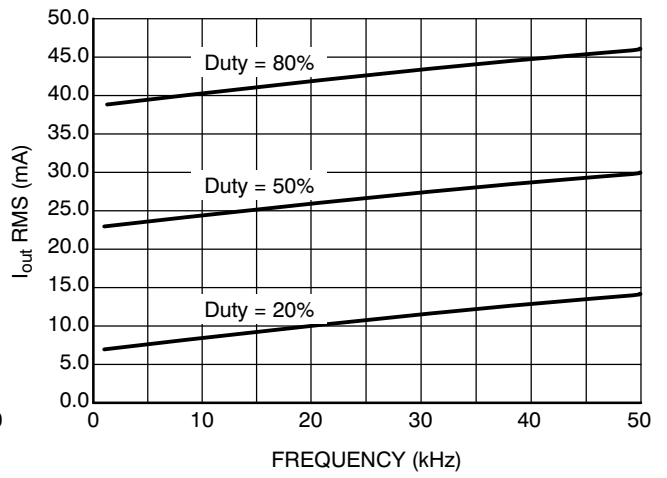


Figure 17. Dimming on CTRL:  $I_{OUT\ RMS}$  vs. Frequency  $R_{BF} = 5\ \Omega$





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internally and provide a phase margin greater than 45° whatever the current supplied or the battery voltage.

### LED Current Selection

Two different currents can be setup by external resistor. The first one is setup by Low Current Sense Resistor ( $R_{LCS}$ ) connected between LCS pin and GND. Usually LCS pin is used to determine the lower current for Torch Mode or indicator mode. The second current is setup by High Current Sense Resistor ( $R_{HCS}$ ) connected between the HCS pin and GND. HCS pin is dedicated setup the current for Flash Mode (see Timeout Section). An active high logic level is applies to CM input,  $R_{HCS}$  resistors is selected when a low level on this pin select the  $R_{LCS}$  resistor. The control loop regulates the current such that the average voltage to HCS or LCS pin is 250 mV (nominal). For example, should one need a 20 mA low output current ( $I_{OUTL}$ ) in the LED branch,  $R_{LCS}$  should be selected according to the following equation:

$$R_{LCS} = \frac{F_{BV}}{I_{outL}} = \frac{250 \text{ mV}}{20 \text{ mA}} = 12.5 \ \Omega \quad (\text{eq. 1})$$

In high current mode ( $I_{OUTH}$ ), when an active high logics level is applies to CM input,  $R_{HCS}$  should be selected according to the following equation:

$$R_{HCS} = \frac{F_{BV}}{I_{outH}} = \frac{250 \text{ mV}}{500 \text{ mA}} = 0.5 \ \Omega \quad (\text{eq. 2})$$

### LED Dimming

In white LED applications it should be desirable to operate the LEDs at a specific operating current because as the biasing current is changed as the color is shifting. As a result of this effect, it should be recommended to fix the maximum current wishes accordingly Equations 1 and 2 and to dim the LED brightness by a pulse width modulation techniques. The PWM signal is applied to CTRL input and thereby the RMS current through LED is proportional to the duly cycle (see Figure 16). In other word by reducing the duty cycle the brightness of the LED is dimmed. The NCP5050 as been design to sustain high PWM dimming frequency up to 50 kHz. Finally to avoid any optical flicker the frequency must be at least higher than 100 Hz.

### Inductor Selection

Three main electrical parameters need to be considered when choosing an inductor: the value of the inductor, the saturation current and the DCR (parasitic serial resistance in DC). Firstly, thank to the high switching frequency at 1.7 MHz (nominal), the NCP5050 allows choosing a low inductor value. This is a key feature mainly in portable application because as inductor value in lower as inductor size in smaller. The recommended inductor value should range from 2.2  $\mu\text{H}$  to 4.7  $\mu\text{H}$ . In one hand higher the inductor value is lower the ripple of current is and in theory better the

efficiency is. But in other hand for a given inductor package size and magnetic material, higher the inductor value is worst the saturation current and DCR are. So a good compromise is to use a 2.7  $\mu\text{H}$  with better DCR possible. Secondly we have to consider the maximum peak current through the inductor ( $I_{PEAK}$ ). Obviously, the peak current inductor is higher when this device supplies the maximum required current so in heavy load conditions. In this case this device is intended to operate in Continuous Conduction Mode (CCM) so the following equation below can be used to calculate the peak current:

$$I_{PEAK} = \frac{I_{out}}{\eta(1-D)} + \frac{V_{in}D}{2LF} \quad (\text{eq. 3})$$

In the equation above,  $V_{IN}$  is the battery voltage,  $I_{OUT}$  is the load current,  $L$  the inductor value,  $F$  the switching frequency, and the duty cycle  $D$  is given by:

$$D = \left(1 - \frac{V_{in}}{V_{out}}\right) \quad (\text{eq. 4})$$

$\eta$  is the global converter efficiency which vary with load current (see Figure 6 though Figure 9). If we select an excessive load current, the global efficiency will be too poor and Power Dissipation ( $P_D$ ) excessive (see Maximum Ratings). A good compromise is to use in worst case  $\eta = 0.75$ . The dotted curve in Figure 20 through Figure 23 gives the inductor peak current as a function of  $I_{OUT}$ , at  $V_{IN} = 3.3 \text{ V}$ , and the number of LEDs in series ( $V_F = 3.5$  typical). It is important to analysis this at worst case conditions to ensure that the inductor current rated is high enough such that it not saturate. So for that refer to the continuous line named "Switch Current Limit Setup by  $R_{PCA}$ " in Figure 20 through Figure 23 that gives peak current which the inductor has to withstand.

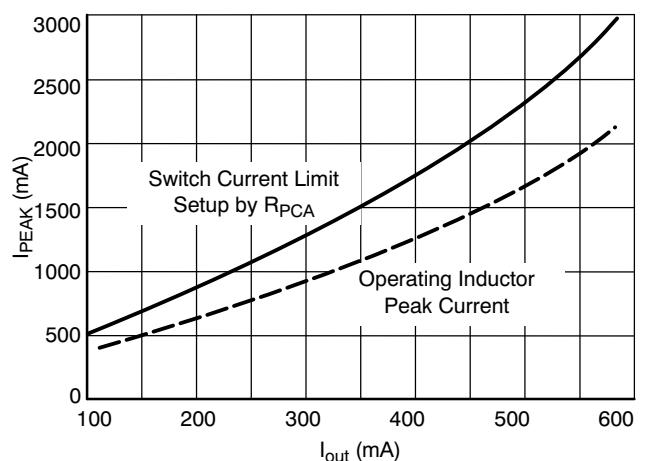
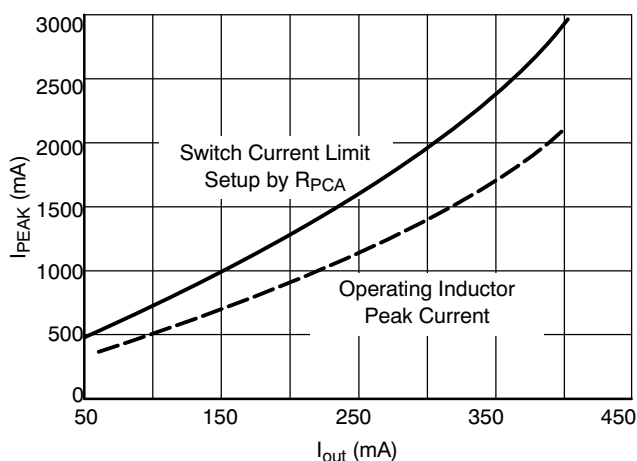
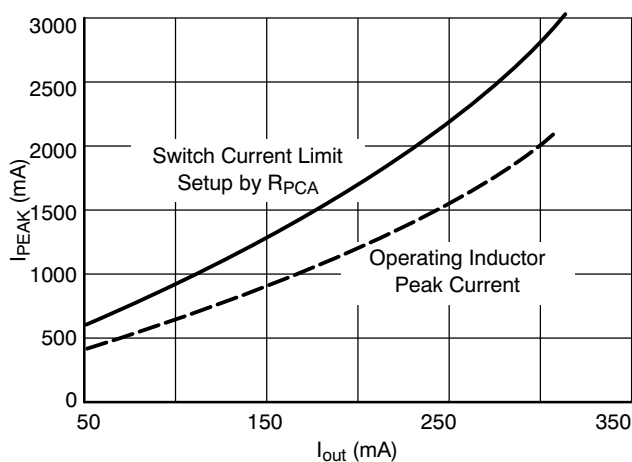


Figure 20. Inductor Peak Currents Vs.  $I_{OUT}$  (mA) for 2 LEDs, (7.0 V @ 350 mA)

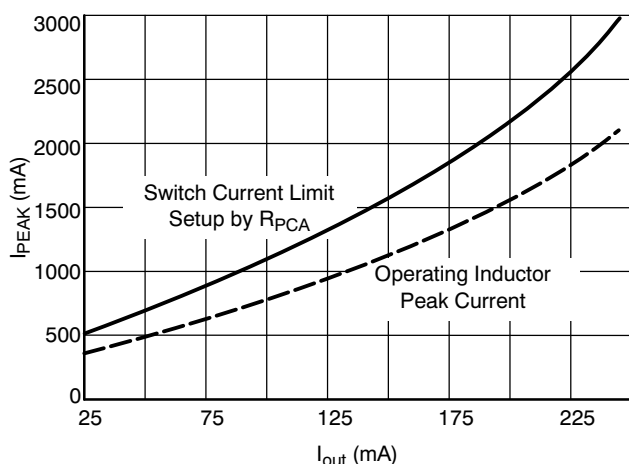
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**Figure 21. Inductor Peak Currents Vs.  $I_{OUT}$  (mA) for 3 LEDs, (10.5 V @ 350 mA)**



**Figure 22. Inductor Peak Currents Vs.  $I_{OUT}$  (mA) for 4 LEDs, (14 V @ 350 mA)**



**Figure 23. Inductor Peak Currents Vs.  $I_{OUT}$  (mA) for 5 LEDs, (17.5 V @ 350 mA)**

Finally, an acceptable DCR must be selected regarding losses in the coil and must be lower than 100 m $\Omega$  to limit excessive voltage drop. In addition, as DCR is reduced,

overall efficiency will improve. Some recommended inductors include but are not limited to:

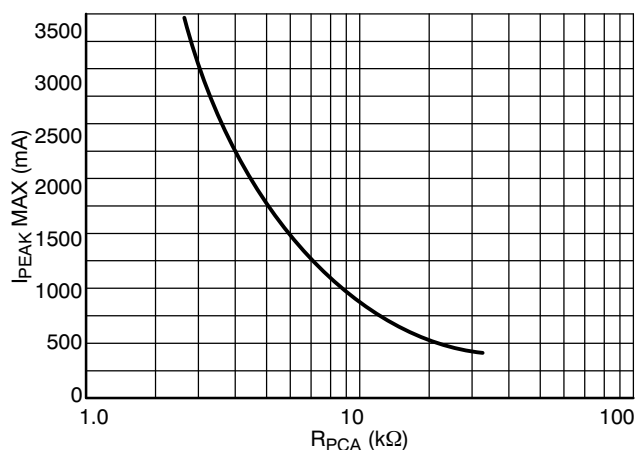
TDK VLF5012A-2R2M1R5  
 TDK VLF5014A-2R7M1R5  
 TDK RLF7030T-3R3M4R1

### Switch Current Limit

This safety feature is clamping the maximum current allowed in the inductor according to external  $R_{PCA}$  resistor, which is connected between PCA input and the ground. This allows the user to reduce the peak current being drawn according to the application's specific requirements. The  $I_{PEAK}$  maximum is 3.0 A, resulting in a minimum resistor value of 2.8 k $\Omega$ . After selecting the switch current limit in section above, please refer to Table 1 or Figure 24 below to choose  $R_{PCA}$  value versus  $I_{PEAK\_MAX}$  accordingly. By limiting the peak current to the needs of the application, the inductor sizing can be scaled appropriately to the specific requirements. This allows the PCB footprint to be minimized.

**Table 1.  $I_{PEAK\_MAX}$  Versus  $R_{PCA}$**

| $I_{PEAK\_MAX}$ (A) | $R_{PCA}$ (k $\Omega$ 1%) |
|---------------------|---------------------------|
| 3.0                 | 2.8                       |
| 2.5                 | 3.4                       |
| 2.0                 | 4.12                      |
| 1.5                 | 5.76                      |
| 1.0                 | 9.09                      |



**Figure 24.  $I_{PEAK\_MAX}$  vs.  $R_{PCA}$**

### Input and Output Capacitors Selection

$C_{OUT}$  stores energy during the  $T_{OFF}$  phase and sustains the load during the  $T_{ON}$  phase. In order ensure the loop stability and minimize the output ripple, at least 1.0  $\mu$ F low ESR multilayer ceramic capacitor type X5R is recommended. Increasing the  $C_{OUT}$  capacitor improved the output voltage ripple.

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The  $P_{VIN}$  input pin need to be bypassed by a X5R or an equivalent low ESR ceramic capacitor. Near the  $P_{VIN}$  pin at least 4.7  $\mu\text{F}$  6.3 V or higher capacitor is needed.

Also a particular care must be observed for DC-bias effects in ceramic capacitor. Actually smaller the case-size and higher the DC bias voltage, the bigger drop in capacitance. For a stability viewpoint the percentage drop in capacitance for the chosen input or output operating voltage must be limit to 20%. Some recommended capacitors include but are not limited to:

1.0  $\mu\text{F}$  25 V 0805

TDK: C2012X5R1E105M

4.7  $\mu\text{F}$  6.3 V 0805

TDK: C1608X5R0J475M

### Schottky Diode Selection

An external diode is required for the boost rectification. The reverse voltage rating of the selected diode must be equal to or greater than the maximum output voltage. The average current rating of the diode must be greater than the maximum output load current. The peak current rating must be larger than the maximum peak inductor current. It is recommended to use a Schottky diode with lower forward voltage to minimize the power dissipation and therefore to maximize the efficiency of the converter.

Also a particular care must be observed for parasitic capacitance versus reverse voltage and leakage current versus junction diode temperature. Both parameters are impacting the efficiency in low load condition and switching quiescent current.

Some recommended Schottky diodes include but are not limited to:

ON SEMICONDUCTOR: MBR130LSFT1G

ON SEMICONDUCTOR: MBR120LSFT3G

### Timeout Protection

To avoid a failure in LEDs caused by a timing violation in Flash Mode (CM high), a timeout function turn off the output after 1.2 second. Any rising edge of CTRL reset this function. In torch mode (CM low) this circuit is disabled. For the logic diagram please refer to Figure 25 below.

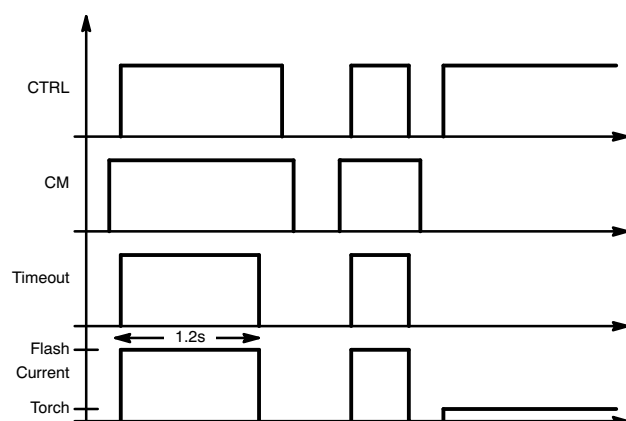


Figure 25. Timeout Operation

### Overvoltage Protection (OVP)

The NCP5050 regulates the load current. If there is an open load condition such as a loose connection to the White LED, the converter keeps supplying current to the  $C_{out}$  capacitor causing the voltage to rise rapidly. To prevent the device from being damage and to eliminate external protections such as zener diode, the NCP5050 incorporates an OVP circuit, which monitors the output voltage with a resistive divider network and a comparator and voltage reference. If the output reaches 22.5 V (nominal), the OVP circuit will detect a fault and inhibit PWM operation. This comparator has 1.0 V of hysteresis so allow the PWM operation to resume automatically. when the load is reconnected and the voltage drops below 21.5 V (nominal).

### Undervoltage Lock Out (UVLO)

To ensure proper operation under all conditions, the device has a built-in undervoltage lock out (UVLO) circuit. During power-up, the device will remain disabled until the input voltage exceeds 2.4 V (nominal). This circuit has 100 mV of hysteresis to provide noise immunity to transient conditions.

### Thermal Considerations

Careful attention must be paid to the internal power dissipation of the NCP5050. The power dissipation is a function of efficiency, input voltage and output power. Hence, increasing the output power requires better components selection. For example, should one change inductors: larger inductor value (in micro Henri) and/or lower DCR may improve efficiency.

The exposed thermal pad that is designed to be soldered to the ground plane to used the PCB as a heat-sink. This ground should then be connected to an internal copper ground plane with thermal via placed directly under the package to spread out the heat dissipated by the device.

Finally the NCP5050 is switched off to protect the device if junction temperature exceeds 160°C. When the junction temperature drops below 140°C, normal operation will resume.

## NCP5050

### ORDERING INFORMATION1

| Device       | Package                     | Shipping†        |
|--------------|-----------------------------|------------------|
| NCP5050MTTXG | WDFN-10 3x3 mm<br>(Pb-Free) | 3000/Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

#### Demo Board Available:

- The NCP5050EVB/D evaluation board that configures the device to drive high current through white LED in serial.

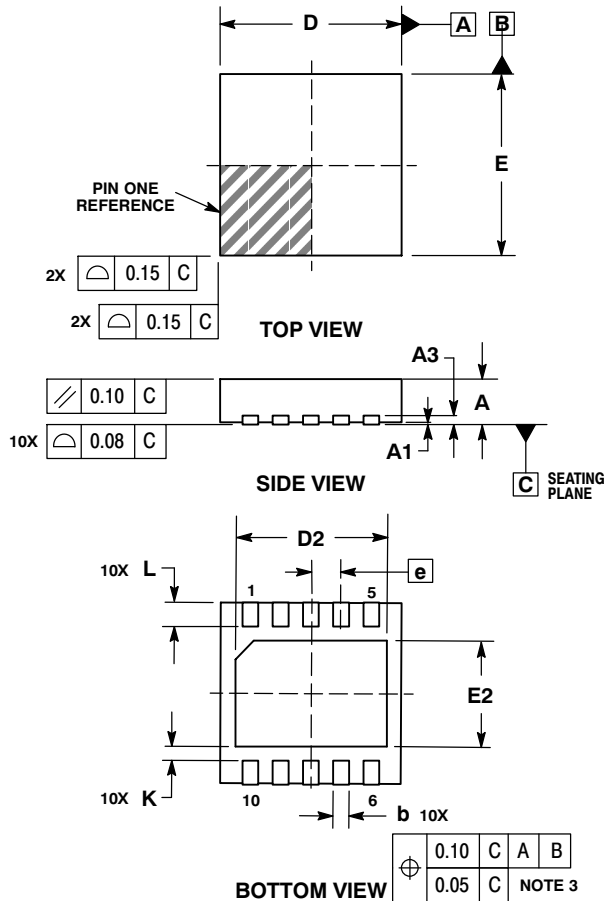
#### Application Note Available:

- AND8294: Drive Up to 120 LEDs (6 to 10 in Series Configuration)

# NCP5050

## PACKAGE DIMENSIONS

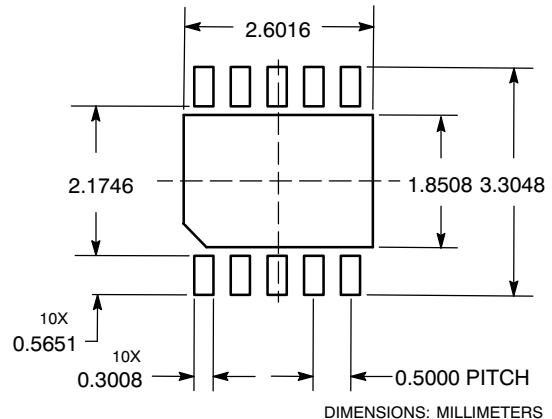
WDFN10, 3x3, 0.5P  
CASE 522AA-01  
ISSUE A



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETERS.
  3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL.
  4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| DIM | MILLIMETERS |      |      |
|-----|-------------|------|------|
|     | MIN         | NOM  | MAX  |
| A   | 0.70        | 0.75 | 0.80 |
| A1  | 0.00        | 0.03 | 0.05 |
| A3  | 0.20 REF    |      |      |
| b   | 0.18        | 0.24 | 0.30 |
| D   | 3.00 BSC    |      |      |
| D2  | 2.45        | 2.50 | 2.55 |
| E   | 3.00 BSC    |      |      |
| E2  | 1.75        | 1.80 | 1.85 |
| e   | 0.50 BSC    |      |      |
| K   | 0.19 TYP    |      |      |
| L   | 0.35        | 0.40 | 0.45 |

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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